



XSIGHT LABS E-SERIES

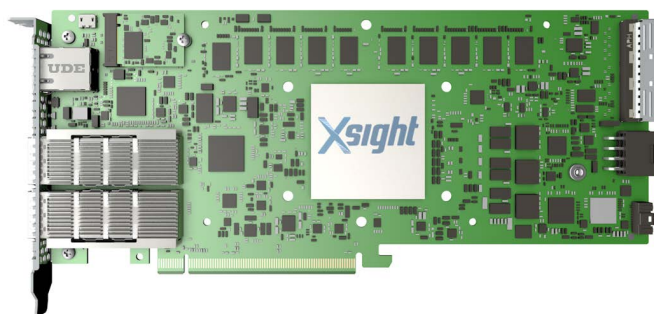
E1 Add-In-Card (AIC)

OVERVIEW

The Xsight Labs E1 Add-In-Card (E1-AIC) is a highly integrated platform for compute, networking, and storage, purpose-built to address the challenges of scaling data centers and AI-driven, compute-intensive applications. Part of the E-Series product family, the E1-AIC redefines performance, efficiency, and adaptability for next-generation infrastructure.

Featuring up to 64 Arm® N2 cores, the E1-AIC delivers 800 Gbps of accelerated networking, wire-speed inline security, advanced storage offloads, and versatile PCIe configurations and connectivity. Its open, standards-based programming model and configurable architecture, including a high-speed coherent interconnect and 32 MB of on-chip RAM, ensure seamless integration and efficient packet processing and support for diverse edge use-cases.

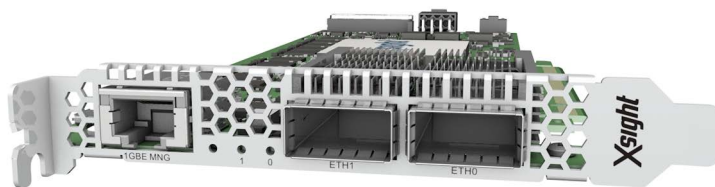
E1-AIC Top View



With a scalable, multi-core architecture that unifies control and data planes, the E1-AIC supports frameworks such as XDP, DPDK, and SPDK, enabling innovation in software-defined networking (SDN), Storage (SDS), security applications, and network infrastructure services. This results in enhanced data center performance, efficiency, and security.

The E1 PCIe Add-In-Card (AIC) is available in a full height three quarter's length (FH3/4L) form factor, tailored for evaluation and deployment in data centers and cloud environments. With support for up to 800 Gbps of network throughput, configuration speeds, such as 2x 400GE, 4x 200GE, or 8x 100GE, the E1-AIC is charged to tackle the challenges of modern data center and AI workloads.

It provides a scalable, high performance, efficient solution for data-intensive operations, making it an essential component of next generation infrastructure.



E1-AIC Front View

DPU DATA CENTER CONSIDERATIONS

In modern data centers, operating systems responsible for virtualization, networking, storage, and security can consume a substantial share of CPU cores and power, reducing the resources available for application workloads. Data Processing Units (DPUs) mitigate this challenge by offloading infrastructure tasks, optimizing resource allocation, and enhancing overall efficiency.

DPUs are particularly valuable in multi-tenant environments, where they provide isolation between server software, virtual machines (VMs), and the data center infrastructure. By managing tasks such as hypervisor operations, DPUs free host CPUs for revenue-generating workloads, improving utilization while enhancing tenant isolation and security.

The Xsight Labs E1-AIC takes a software-defined approach, offering compatibility with open-source solutions and programmability for diverse applications. Designed for seamless integration with existing ecosystems, the E1-AIC enables advanced features such as PCIe-emulated devices for virtualized networking and storage interfaces, while supporting up to 800 Gbps throughput. When selecting a DPU, factors such as interoperability, maintainability, flexibility, and application integration are as critical as performance for successful deployment.

DPU AI NETWORKING CONSIDERATIONS

As AI workloads grow in complexity and scale, modern data centers face increasing demands on networking infrastructure to ensure optimal performance, efficiency, and scalability. DPUs address these challenges by offloading front-end networking and infrastructure management tasks from the host CPU, enabling resources to focus on AI compute-intensive applications, while ensuring the isolation and security required in modern data centers.

In AI backend networking, DPUs are critical for achieving high throughput and low latency communication across distributed training and inference clusters. They improve data flow efficiency by accelerating packet processing,

optimizing data movement, and delivering consistent performance during heavy or bursty workloads. Advanced features such as congestion management and traffic shaping ensure balanced performance in high-bandwidth environments, crucial for AI workloads.

The software-defined architecture of the E1-AIC enhances support for diverse AI workloads by seamlessly integrating with existing systems and enabling flexible programmability. By accelerating networking and optimizing data center infrastructure, the E1-AIC equips data centers to meet the rigorous demands of next-generation AI workloads while maintaining efficiency and scalability.

DPU BUMP-IN-THE-WIRE CONSIDERATIONS

Bump-in-the-wire deployments require DPUs to efficiently manage networking, security, and infrastructure workloads with minimal latency. These deployments demand a balance between hardware performance and software programmability to address the diverse and evolving needs of modern data centers. Traditional DPUs relying heavily on hardware-based offloads often lack the computational flexibility needed to support software-defined networking (SDN) environments.

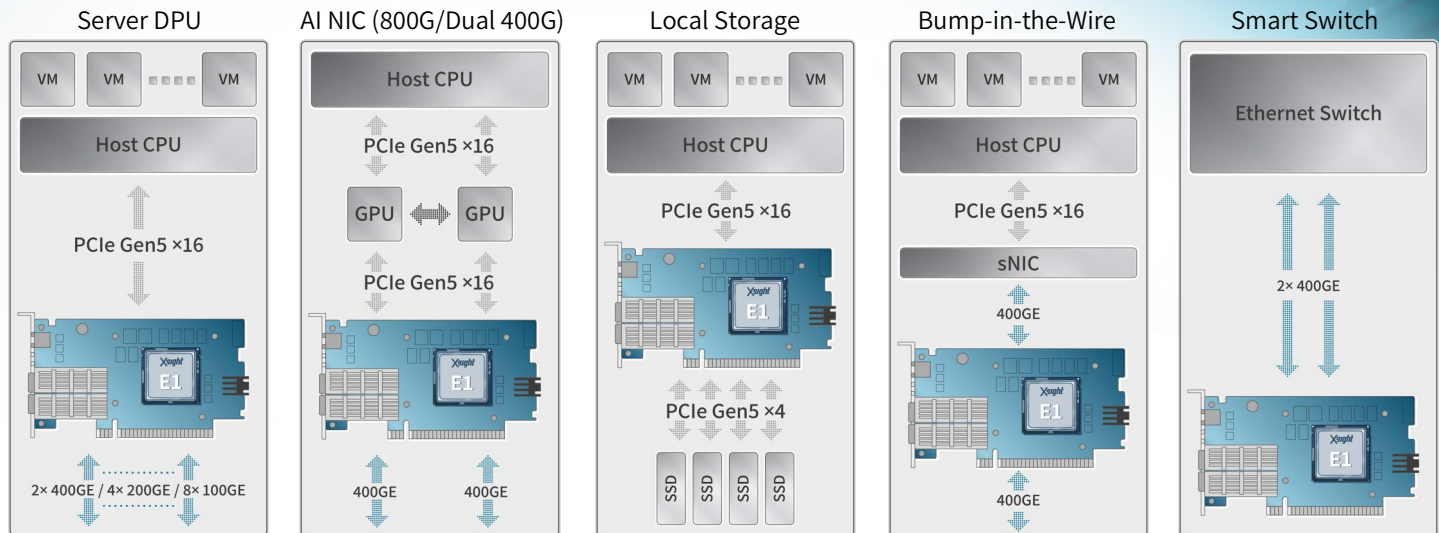
The E1-AIC addresses these challenges with its software-defined architecture, powered by 64 Arm N2 cores, providing the computational agility and performance needed for complex,

dynamic workloads. Its architecture enables high-throughput operations while maintaining the flexibility to adapt to changing requirements. For instance, in SONiC-DASH (Disaggregated API for SONiC Hosts), the E1-AIC efficiently processes SDN flow workloads at 800 Gbps, tackling the growing need for scalable stateful flow processing in modern data centers.

This software-driven approach allows customers to standardize their software stack across platforms, providing seamless integration, scalability, and adaptability for diverse deployment scenarios.

TARGET APPLICATIONS

- Multi-host optimized Smart-NIC with flexible buffering
- AI/ML/HPC RDMA
- Smart Switch DPU architectures supporting
 - + Up to 400 Mpps bi-directional
 - + 20M connections per second
- Data path offload for virtual switching in bump-in-wire configurations
- Full hyper-visor offload and bare metal provisioning
- Full stack offload for NVMe-oF and NVMe/TCP storage initiator and target
- TLS/DTLS Termination with TCP and QUIC Proxy
- Scalable, full-featured TLS/kTLS offload
- Stateful distributed firewall architectures
- Local/remote storage connectivity



E1 SOC FEATURES

Compute and Memory

- 64 Arm Neoverse™ N2 v9.0-A cores
- 32MB of internal RAM, presented as System Level Cache or direct-mapped memory, with NUMA and MPAM support.
- 4 DDR5 at 5200 MT/s
- Inline AES-XTS memory encryption
- High Speed coherent interconnect

Programmable PCIe Fabric

- 32 PCIe Gen5.0 lanes
- Endpoint and Root-port functionality per PCIe link
- PCIe configuration space emulation
- Software-based MMIO space emulation
- SR-IOV with up to 64K PF/VFs and scalable IOV
- Multi-host support
- Peer-to-peer PCIe switching with address translation

Accelerated Networking, Storage and Security

- 2x400G, 4x200G or 8x100G/50G/25G/10G port configurations
- Protocol-independent programmable parser and multi-stage exact match lookup with DRAM-backed tables
- Line rate AES-GCM network crypto supporting IPsec ESP and UDP SEC
- Software-activated 3 Tbps DMA engines with cache stashing
- Stateless offloads: Checksum, RSS, TSO, RoCEv2 iCRC
- Line rate block storage crypto with AES-XTS
- Storage Protection Information offloads including T10-DIF/DIX, CRC GMAC and SHA2/3, and scrub CRC

Open, Standards-based, Extensible Software

- Arm-based firmware processor with UEFI secure boot, HW root-of-trust
- UEFI Secure boot with Arm Trusted Firmware (TF-A)
- Arm SystemReady™ certification for running unmodified Linux distros
 - + Debian, Ubuntu, SONiC
- Linux Netdev, VirtIO and Xsight Network Adapter (XNA) drivers
- Custom SDN data planes with Linux, XDP and DPDK/SPDK programming models
- Infrastructure software and reference applications
 - + SONiC with DASH data plane
 - + Virtual Switch
 - + RoCEv2

E1-AIC KEY FEATURES

Feature	Description
Network	800 Gb/s Ethernet connectivity with two QSFP112 connectors Examples of supported port configurations: • 2x 400G using 8x 100G lanes • 1x 400G using 8x 50G lanes • 2x 200G using 8x 50G lanes • 2x 100G using 8x 25G lanes
Connectivity	Two ports PCIe Gen5.0 x16 interfaces • CEM Edge Connector (PCIe End-Point) • MCIO connector right angle (PCIe Root-Port/End-Point) + MCIO to SSD midplane + MCIO to edge for supporting two hosts with one card
Memory	32 GB or 64 GB on-board DDR5-5200 (2 interfaces, 83.2 GB/s), implemented with twenty x8 DRAM devices (ECC supported).
Storage	• M.2 SSD 128 GB • 64 MB NOR Flash
Management	Support control, configuration, and diagnostics: • Single RJ45 port with integrated LEDs, serving as a management interface to provide network connectivity for control and monitoring. • I2C/SMBus: Network Communication via edge and MCIO connectors • PCIe PLDM: Over either I2C or PCIe. • Firmware Upgrade: Supports non-BMC mechanisms, including UEFI and Linux-secure capsule for secure firmware updates. • NC-SI via 20-pin connector - HW ready
Security	• Hardware-based TPM 2.0 • Secure Boot • Hardware Root of Trust
Temperature	• Temperature sensor
Form Factor	Full-height, 3/4-length (FH3/4L) PCIe add-in card for data center and cloud applications.
Real Time Clock (RTC)	On-board RTC with a super-cap for up to two days of data protection. Note: Super-cap is limited to indoor use-cases only at temperatures under 60°C.
Timing	• 1PPS MMCX connector for Inputs • 1PPS MMCX connector for Outputs
Power Supply	Power is supplied through two connectors • 12V from CEM connector: up to 75W • 12V from Auxiliary 8-pin connector: up to 150W
Thermal	Heat sink vapor chamber heat sink

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